

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2001-250396**

(43)Date of publication of application : **14.09.2001**

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(51)Int.Cl. **G11C 29/00**

**G01R 31/28**

**G11C 17/00**

**H01L 21/66**

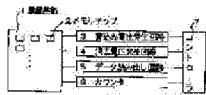
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**(54) SCREENING METHOD FOR NON-VOLATILE SEMICONDUCTOR  
MEMORY AND ITS DEVICE**



(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method and a device which can perform screening simply and quickly without requiring special technology.

SOLUTION: In this screening method for a non-volatile semiconductor memory, an initial erasing time  $tei$  in which written data is erased in an initial state is measured, it is compared with a set erasing time  $tes$  previously set, and pass/fail is discriminated. A set erasing time is set based on the following relation. That is, plural memory chips are sampled, write-in voltage from a write-in voltage generating circuit 3 and erasing voltage from an erasing voltage generating circuit 4 are repeatedly applied to plural memory chips 2, the number of times of being erasable  $Nf$  immediately before disablement of erasion is measured and relation between the initial erasing time and the number of times of being erasable is grasped.

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LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's  
decision of rejection]

[Kind of final disposal of application  
other than the examiner's decision of  
rejection or application converted  
registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's  
decision of rejection]

[Date of requesting appeal against  
examiner's decision of rejection]

[Date of extinction of right]

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## CLAIMS

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[Claim(s)]

[Claim 1] The screening approach of the non-volatile semiconductor memory characterized by judging success or failure as compared with the setting blanking time (tes) which measured the blanking time (te) which eliminates said written-in data in the screening approach of the non-volatile semiconductor memory in which the writing and elimination of data are possible, and was set up beforehand.

[Claim 2] The screening approach of the non-volatile semiconductor memory according to claim 1 which is the initial blanking time (tei) by which said blanking time was measured by the initial state.

[Claim 3] Said setting blanking time is the screening approach of the non-volatile semiconductor memory according to claim 1 or 2 which samples two or more

memory chips, measures an eliminable count (Nf) just before writing in said two or more memory chips, repeating and impressing an electrical potential difference and blanking voltage and eliminating becoming impossible, grasps the relation between said initial blanking time and said eliminable count, and is decided based on this relation.

[Claim 4] The installation substrate which lays two or more sampled memory chips, and the write-in electrical-potential-difference generating circuit which generates the write-in electrical potential difference impressed to said two or more memory chips, The blanking voltage generating circuit which similarly generates blanking voltage, and the data readout circuitry which reads an elimination signal, The counter which measures the count of impression of said blanking voltage, or the count of read-out of said elimination signal, Screening equipment of the non-volatile semiconductor memory characterized by computing an eliminable count (Nf) and said blanking time just before having the controller which controls said a series of circuits, repeating and impressing a write-in electrical potential difference and said blanking voltage and eliminating becoming impossible.

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**DETAILED DESCRIPTION**

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the screening approach of the non-volatile semiconductor memory currently used for the industrial control equipment, the computer, etc., and its equipment.

[0002]

[Description of the Prior Art] It is a certain threshold electrical potential difference  $V_{th0}$  as one of the screening approaches which secures reliable non-volatile semiconductor memory conventionally. There was a method of judging the above non-volatile semiconductor memory to be a normal article. Namely, threshold electrical potential difference [ in / using the sample of the number of specification extracted from the memory chip for evaluation at random as shown in drawing 7 / non-volatile semiconductor memory ]  $V_{th0}$  It is a certain threshold electrical potential difference  $V_{th0}$  to all the products that create and screen a histogram. The above non-volatile semiconductor memory was judged to be a normal article.

[0003]

[Problem(s) to be Solved by the Invention] However, by the conventional screening approach, in order to measure the threshold of the whole flash plate memory chip and to use a special static test mode, it is necessary to grasp special techniques, such as hardware architecture of non-volatile semiconductor memory, and, and there was a problem that the whole screening system was complicated and measurement took time amount. Then, this invention does not need a special technique but it aims at offering the approach and equipment which can be screened simply quickly.

[0004]

[Means for Solving the Problem] In order to solve the above-mentioned problem, this invention is good to measure the blanking time ( $t_e$ ) which eliminates said written-in data, to make it the configuration which judges success or failure as

compared with the setting blanking time (tes) set up beforehand, and to make it the initial blanking time (tei) by which said blanking time was measured by the initial state in the screening approach of the non-volatile semiconductor memory in which the writing and elimination of data are possible. Moreover, said setting blanking time samples two or more memory chips, measures an eliminable count (Nf) just before writing in said two or more memory chips, repeating and impressing an electrical potential difference and blanking voltage and eliminating becoming impossible, grasps the relation between said initial blanking time and said eliminable count, and is decided based on this relation. Moreover, the screening equipment of the non-volatile semiconductor memory of this invention The installation substrate which lays two or more sampled memory chips, and the write-in electrical-potential-difference generating circuit which generates the write-in electrical potential difference impressed to said two or more memory chips, The blanking voltage generating circuit which similarly generates blanking voltage, and the data readout circuitry which reads an elimination signal, The counter which measures the count of impression of said blanking voltage, or the count of read-out of said elimination signal, It has the controller which controls said a series of circuits, a write-in electrical potential difference and said blanking voltage are repeated and impressed, and it is made the configuration which computes an eliminable count (Nf) and said blanking time just before eliminating becomes impossible.

[0005]

[Embodiment of the Invention] Hereafter, the example of this invention is explained to a detail based on drawing. Drawing 1 is the block diagram showing the screening equipment of the non-volatile semiconductor memory of this invention. In drawing, the installation substrate with which 1 lays the memory chip 2 for screening, the data readout circuitry to which a write-in electrical-potential-difference generating circuit and 4 measure a blanking voltage generating circuit, and, as for 5, 3 measures blanking time, the counter with which 6 measures the count of read-out, and 7 are controllers which control a series of circuits. The

cellular structure of the non-volatile semiconductor memory of a memory chip 1 is shown in the mimetic diagram of drawing 2 , (a) shows the conceptual diagram of the cellular structure and (b) shows the conceptual diagram of a memory array. For 21, as for a drain and 23, in drawing, Si substrate and 22 are [ the source and 24 ] oxide films. In addition, in VG, a word line and VS show a source line and VD shows a bit line. The cellular structure of a memory chip 2 is the thing of the flash memory of the capacity 128KB type which writes in and eliminates data with a Floating gate Thin Oxide mold by Fowler-Nordheim Tunneling (it abbreviates to F-N Tunneling hereafter). In the conceptual diagram of drawing 2 (b), four memory cells have been arranged, in the control gate of a cel, a bit line is arranged for a word line, the source line is arranged to the drain at the source, and the above-mentioned wiring is arranged in the  $1024 \times 128 \times 8 = 1048576$  piece cel. The electrical potential difference impressed at the time of data writing, elimination, and verification is shown in Table 1.

[0006]

[Table 1]

	$V_c/V$	$V_b/V$	$V_s/V$
書き込み	10	6	0
読み込み	4.75	1	0
ペリファイ	2.7	0	8.2

[0007] Actuation is described below. Screening was performed according to the flow chart shown in drawing 3 . First, 12 flash memories were prepared as a sample. Blanking time te It measured by the approach of showing relation with the count N of elimination in drawing 4 . Drawing 4 is the eliminable count Nf. And it is the flow chart of the measurement algorithm of blanking time te. Eliminable count Nf It is loop count N of drawing 3 , and is blanking time te. It defines, the product, i.e.,  $te = mxtes$ , of the set-up blanking time (it abbreviates to the setting blanking time tes hereafter), and loop count m of elimination. The measurement result of three typical samples is shown in drawing 5 among 12 samples. The initial blanking time tei is the first blanking time te from

measurement initiation. The definition was given. Blanking time  $t_e$  It decreases in early stages of writing and elimination, is stabilized after that, and is in the inclination which increases rapidly [ just before writing and elimination become impossible ]. Moreover, the long sample of the initial blanking time  $t_{ei}$  is the eliminable count  $N_f$ . It is few and the short sample of the initial blanking time  $t_{ei}$  is the eliminable count  $N_f$ . Many Furthermore, as shown in drawing 6 , they are the initial blanking time  $t_{ei}$  and the eliminable count  $N_f$ . Data were approximated with the least square method and the curve fit was carried out. A continuous line shows the curve fit itself, the wavy line shows the confidence interval, and this created the master curve. It is  $N_f$  about the desired value of writing / elimination resistance which a flash memory user demands now. If it is a time, normal blanking time will serve as  $t_{ec}$  from the master curve of drawing 5 . Therefore, it is  $N_f$  by measuring the initial blanking time  $t_{ei}$  and screening the flash memory which becomes  $t_{ei} < t_{ec}$  as a normal article to the flash plate memory chip total which a user uses. The writing and elimination more than a time are guaranteed. With an above-mentioned approach and equipment, when the flash memory was screened, it was able to screen in large quantities and correctly only by measuring the initial blanking time  $t_{ei}$  in a short time. In addition, although this example had taken up the flash memory as non-volatile semiconductor memory, the good result was similarly obtained about EEPROM.

[0008]

[Effect of the Invention] Since it was made the configuration which judges success or failure as compared with the setting blanking time which measured the blanking time which eliminates the written-in data by the initial state, and was set up beforehand according to this invention as stated above, a special technique is not needed but a lot of non-volatile semiconductor memory can be screened in a short time. For this reason, it is effective in reliable non-volatile semiconductor memory being correctly securable.

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**DESCRIPTION OF DRAWINGS**

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**[Brief Description of the Drawings]**

[Drawing 1] It is the block diagram showing the screening equipment of the non-volatile semiconductor memory of this invention.

[Drawing 2] It is drawing showing the cellular structure of the non-volatile semiconductor memory used for this invention, and (a) shows the conceptual diagram of the cellular structure and (b) shows the conceptual diagram of a memory array.

[Drawing 3] It is the flow chart which shows the screening approach of this invention.

[Drawing 4] It is the flow chart which measures the eliminable count and blanking time of this invention.

[Drawing 5] It is the graph which shows the blanking time of this invention, and the measurement result of the count of elimination.

[Drawing 6] It is the graph which shows the relation between the eliminable count of this invention, and blanking time.

[Drawing 7] It is the histogram of the non-volatile semiconductor memory which used the threshold electrical potential difference which is the conventional screening approach.

**[Description of Notations]**

- 1: Installation substrate
- 2: Memory chip
- 3: Write-in electrical-potential-difference generating circuit
- 4: Blanking voltage generating circuit
- 5: Data readout circuitry
- 6: Counter
- 7: Controller

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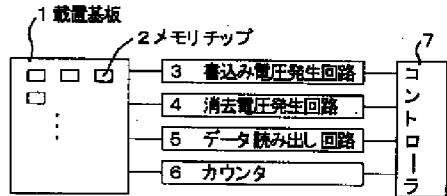
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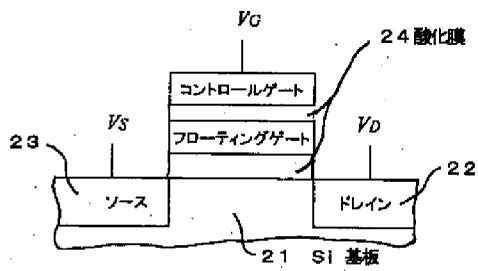
## DRAWINGS

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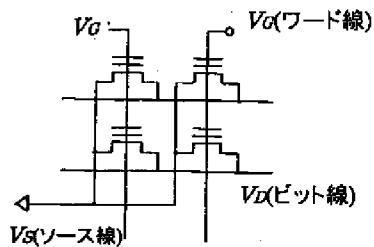
[Drawing 1]



[Drawing 2]

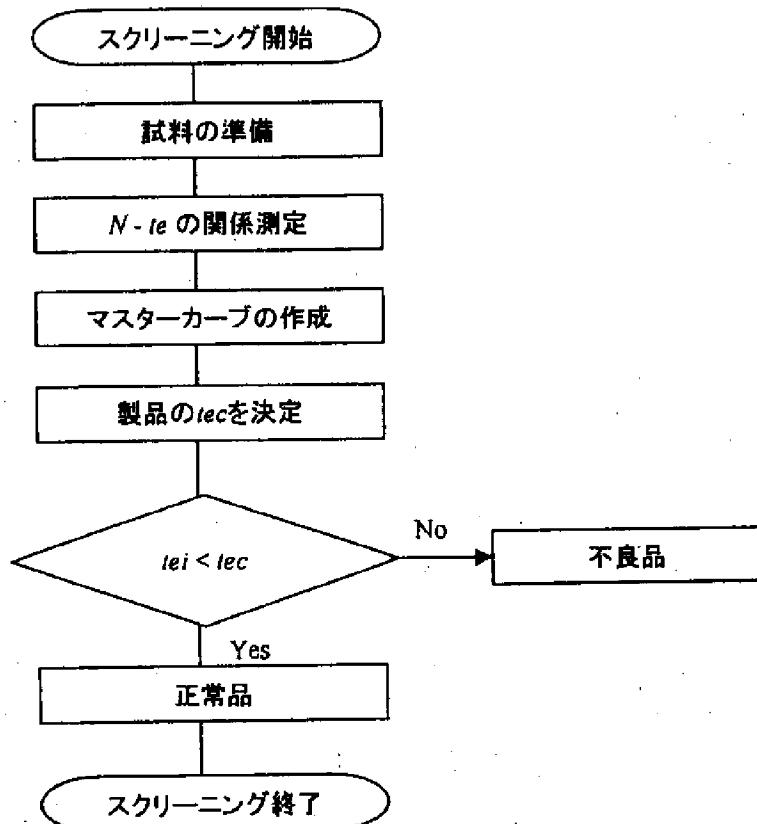


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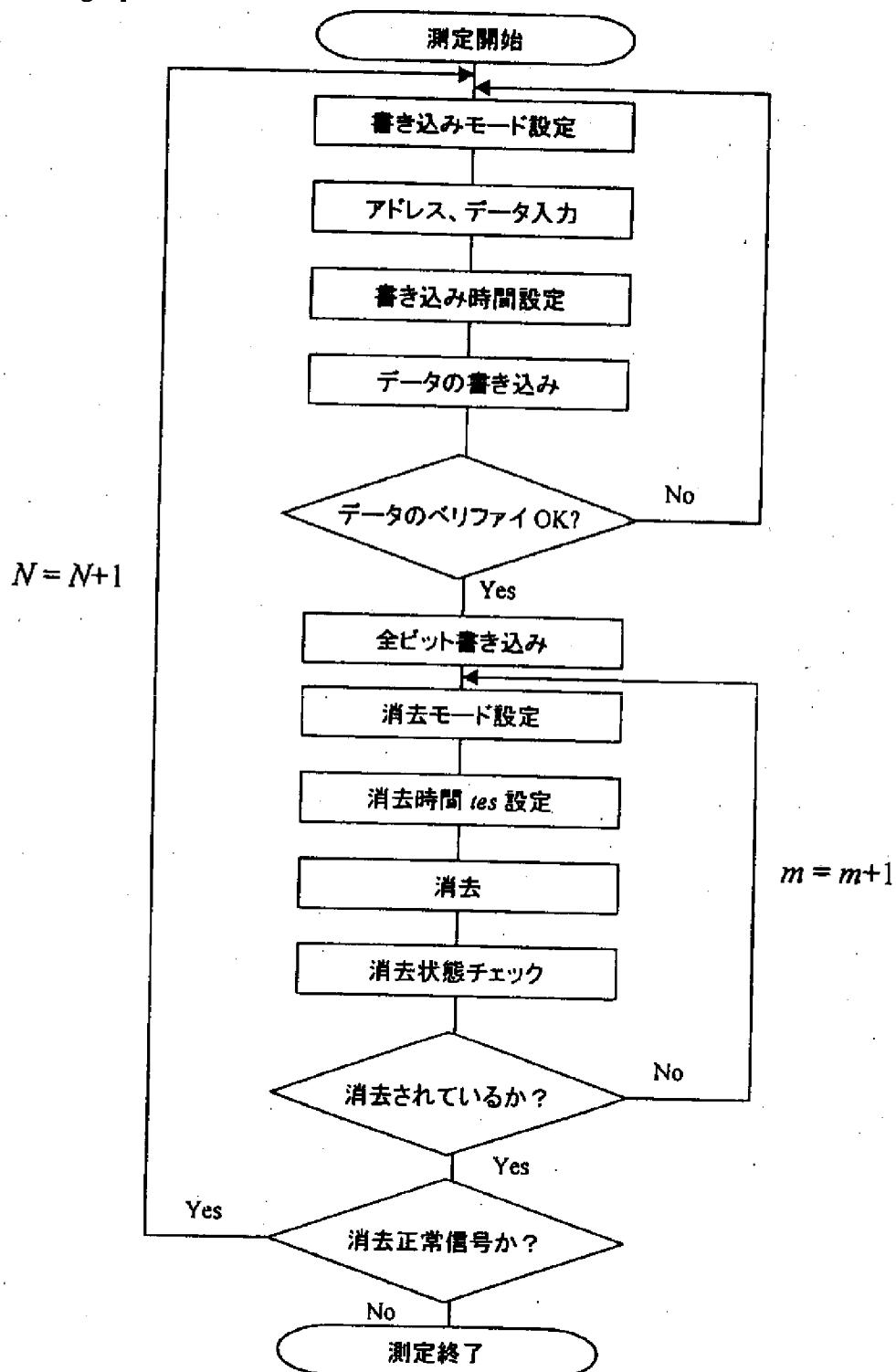


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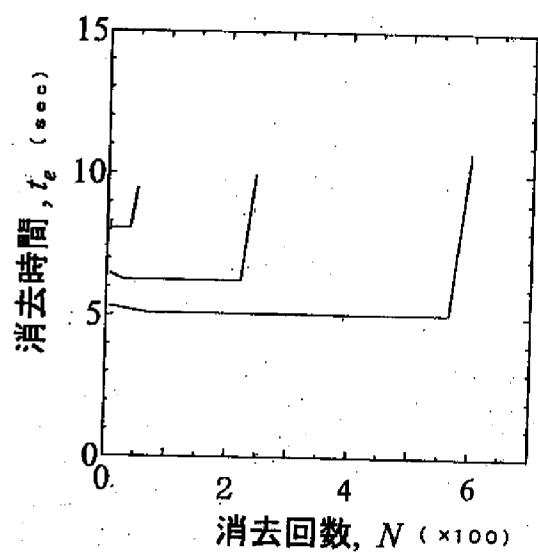
[Drawing 3]



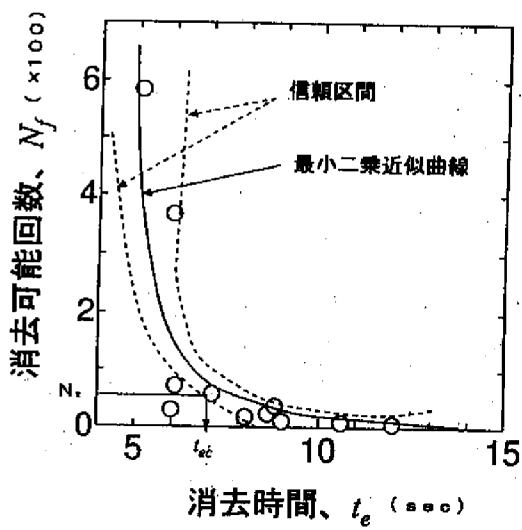
[Drawing 4]



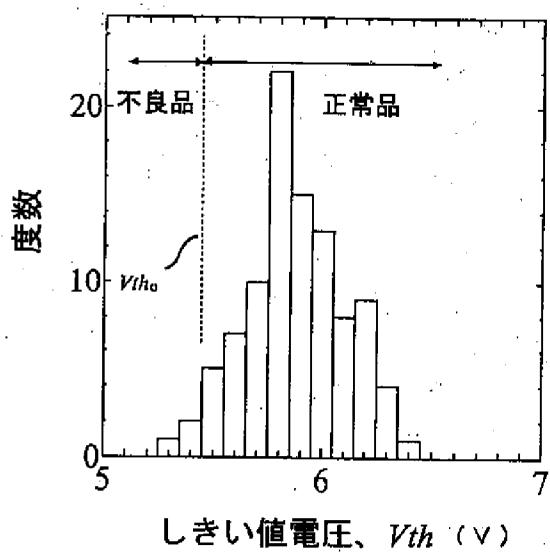
[Drawing 5]



[Drawing 6]



[Drawing 7]



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(19)日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開2001-250396

(P2001-250396A)

(43)公開日 平成13年9月14日 (2001.9.14)

(51)Int.Cl. <sup>7</sup>	識別記号	F I	テ-マコ-ト <sup>8</sup> (参考)
G 1 1 C 29/00	6 5 2	C 1 1 C 29/00	6 5 2 2 G 0 3 2
G 0 1 R 31/28		17/00	D 4 M 1 0 6
G 1 1 C 17/00		H 0 1 L 21/66	W 5 B 0 0 3
H 0 1 L 21/66		G 0 1 R 31/28	B 5 L 1 0 6
			9 A 0 0 1

審査請求 未請求 請求項の数4 O L (全 6 頁)

(21)出願番号 特願2000-59809(P2000-59809)

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(22)出願日 平成12年3月6日 (2000.3.6)

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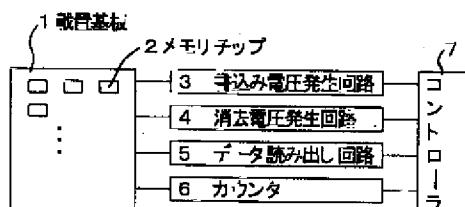
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(54)【発明の名称】 不揮発性半導体メモリのスクリーニング方法およびその装置

(57)【要約】

【課題】特別な技術を必要とせず、簡単でかつ迅速にスクリーニングできる方法および装置を提供する。

【解決手段】本発明の不揮発性半導体メモリのスクリーニング方法は、書き込まれたデータを初期状態で消去する初期消去時間( $t_{ei}$ )を測定し、予め設定した設定消去時間( $t_{es}$ )と比較して合否を判定するもので、設定消去時間は、複数のメモリチップ2に書き込み電圧発生回路3からの書き込み電圧と消去電圧発生回路4からの消去電圧を繰り返し印加して消去不能となる直前の消去可能回数( $N_f$ )を計測し、初期消去時間と消去可能回数の関係を把握し、この関係を基に設定する。



**【特許請求の範囲】**

【請求項1】データの書き込みおよび消去が可能な不揮発性半導体メモリのスクリーニング方法において、前記書き込まれたデータを消去する消去時間( $t_e$ )を測定し、予め設定した設定消去時間( $t_{es}$ )と比較して合否を判定することを特徴とする不揮発性半導体メモリのスクリーニング方法。

【請求項2】前記消去時間が初期状態で計測された初期消去時間( $t_{ei}$ )である請求項1記載の不揮発性半導体メモリのスクリーニング方法。

【請求項3】前記設定消去時間は、複数のメモリチップをサンプリングし、前記複数のメモリチップに書き込み電圧と消去電圧を繰り返し印加して消去不能となる直前の消去可能回数( $N_f$ )を計測し、前記初期消去時間と前記消去可能回数の関係を把握し、この関係を基にして決める請求項1または2記載の不揮発性半導体メモリのスクリーニング方法。

【請求項4】サンプリングした複数のメモリチップを載置する載置基板と、前記複数のメモリチップに印加する書き込み電圧を発生する書き込み電圧発生回路と、同じく消去電圧を発生する消去電圧発生回路と、消去信号を読み出すデータ読み出し回路と、前記消去電圧の印加回数または前記消去信号の読み出し回数を計測するカウンターと、前記一連の回路を制御するコントローラとを備え、書き込み電圧と前記消去電圧を繰り返し印加し、消去不能となる直前の消去可能回数( $N_f$ )および前記消去時間を算出することを特徴とする不揮発性半導体メモリのスクリーニング装置。

**【発明の詳細な説明】****【0001】**

【発明の属する技術分野】本発明は、産業用制御機器およびコンピュータ等に使用されている不揮発性半導体メモリのスクリーニング方法およびその装置に関する。

**【0002】**

【従来の技術】従来、信頼性の高い不揮発性半導体メモリを確保するスクリーニング方法の一つとして、あるしきい値電圧 $V_{th0}$ 以上の不揮発性半導体メモリを正常品と判断する方法があった。すなわち、図7に示すように、評価対象のメモリチップから無作為に抽出した特定数の試料を用いて不揮発性半導体メモリにおけるしきい値電圧 $V_{th0}$ のヒストグラムを作成し、スクリーニングする全製品に対して、あるしきい値電圧 $V_{th0}$ 以上の不揮発性半導体メモリを正常品と判断していた。

**【0003】**

【発明が解決しようとする課題】ところが、従来のスクリーニング方法では、フラッシュメモリチップ全体のしきい値を測定するには、特殊なテストモードを使用するため、不揮発性半導体メモリのハードウェアーアーキテクチャー等の特殊な技術を把握している必要があり、また、スクリーニングシステム全体が複雑で測定に時間が

かかるという問題があった。そこで、本発明は特別な技術を必要とせず、簡単かつ迅速にスクリーニングできる方法および装置を提供することを目的とする。

**【0004】**

【課題を解決するための手段】上記問題を解決するため、本発明は、データの書き込みおよび消去が可能な不揮発性半導体メモリのスクリーニング方法において、前記書き込まれたデータを消去する消去時間( $t_e$ )を測定し、予め設定した設定消去時間( $t_{es}$ )と比較して合否を判定する構成にしており、前記消去時間が初期状態で計測された初期消去時間( $t_{ei}$ )にするとよい。また、前記設定消去時間は、複数のメモリチップをサンプリングし、前記複数のメモリチップに書き込み電圧と消去電圧を繰り返し印加して消去不能となる直前の消去可能回数( $N_f$ )を計測し、前記初期消去時間と前記消去可能回数の関係を把握し、この関係を基にして決められる。また、本発明の不揮発性半導体メモリのスクリーニング装置は、サンプリングした複数のメモリチップを載置する載置基板と、前記複数のメモリチップに印加する書き込み電圧を発生する書き込み電圧発生回路と、同じく消去電圧を発生する消去電圧発生回路と、消去信号を読み出すデータ読み出し回路と、前記消去電圧の印加回数または前記消去信号の読み出し回数を計測するカウンターと、前記一連の回路を制御するコントローラとを備え、書き込み電圧と前記消去電圧を繰り返し印加し、消去不能となる直前の消去可能回数( $N_f$ )および前記消去時間を算出する構成にしている。

**【0005】**

【発明の実施の形態】以下、本発明の実施例を図に基づいて詳細に説明する。図1は、本発明の不揮発性半導体メモリのスクリーニング装置を示すブロック図である。図において、1はスクリーニング対象のメモリチップ2を載置する載置基板、3は書き込み電圧発生回路、4は消去電圧発生回路、5は消去時間を測定するデータ読み出し回路、6は読み出し回数を計測するカウンタ、7は一連の回路を制御するコントローラである。メモリチップ1の不揮発性半導体メモリのセル構造は、図2の模式図に示すようになっており、(a)はセル構造の概念図を、(b)はメモリアレイの概念図を示している。図において、21はSi基板、22はドレイン、23はソース、24は酸化膜である。なお、VGはワード線、VSはソース線、VDはビット線を示す。メモリチップ2のセル構造は、Floating gate Thin Oxide型でFowler-Nordheim Tunneling(以下、F-N Tunnelingと略す)でデータを書き込み・消去する容量128KBタイプのフラッシュメモリのものである。図2(b)の概念図では、4つのメモリセルを配置し、セルのコントロールゲートにはワード線を、ドレインにはビット線を、ソースにソース線を配置しており、 $1024 \times 128 \times 8 = 1048576$ 個のセルに、上記配線を配置している。表1にデータ書き込み・消去、

ペリファイ時に印加する電圧を示す。

【0006】

【表1】

	$V_e/V$	$V_p/V$	$V_s/V$
書き込み	10	6	0
読み込み	4.75	1	0
ペリファイ	2.7	0	8.2

【0007】つぎに動作について述べる。スクリーニングは、図3に示すフローチャートに従って行った。最初に、12個のフラッシュメモリを試料として準備した。消去時間 $t_e$ と消去回数 $N$ との関係を図4に示す方法により測定した。図4は消去可能回数 $N_f$ および消去時間 $t_e$ の測定アルゴリズムのフローチャートである。消去可能回数 $N_f$ は図3のループ回数 $N$ で、消去時間 $t_e$ は設定した消去時間(以下、設定消去時間 $t_{es}$ と略す)と消去のループ回数 $m$ との積、すなわち、 $t_e = m \times t_{es}$ と定義する。12個のサンプル中、代表的な3試料の測定結果を図5に示す。初期消去時間 $t_{ei}$ は、測定開始から第一回目の消去時間 $t_e$ で定義した。消去時間 $t_e$ は、書き込み・消去の初期に減少し、その後安定し、書き込み・消去が出来なくなる直前に急激に増加する傾向にある。また、初期消去時間 $t_{ei}$ の長い試料は消去可能回数 $N_f$ が少なく、初期消去時間 $t_{ei}$ の短い試料は消去可能回数 $N_f$ が多い。さらに、図6に示すように初期消去時間 $t_{ei}$ と消去可能回数 $N_f$ とのデータを、最小二乗法により近似してカーブフィットした。実線はカーブフィットそのものを、波線は信頼区間を示しており、これによりマスターカーブを作成した。今、フラッシュメモリユーザの要求する書き込み・消去耐性の目標値を $N_f$ 回とすると、図5のマスターカーブより、正常消去時間は $t_{ec}$ となる。したがって、ユーザが使用するフラッシュメモリチップ全数に対して、初期消去時間 $t_{ei}$ を測定し、 $t_{ei} < t_{ec}$ になるフラッシュメモリを正常品としてスクリーニングすることにより、 $N_f$ 回以上の書き込み・消去は保証される。上述の方法および装置により、フラッシュメモリをスクリーニングすると初期消去時間 $t_{ei}$ を測定するのみで、短時間で大量にかつ正確にスクリーニングすることができた。なお、本実施例は、不揮発性半導体メモリとして、フラッシュメモリを取り上げているが、EEPROMについても同様に良好な結果が得られた。

【0008】

【発明の効果】以上述べたように本発明によれば、書き込まれたデータを初期状態で消去する消去時間を測定し、予め設定した設定消去時間と比較して合否を判定する構成にしたので、特別な技術を必要とせず、短時間に大量の不揮発性半導体メモリをスクリーニングできる。このため信頼性の高い不揮発性半導体メモリを正確に確保できる効果がある。

【図面の簡単な説明】

【図1】本発明の不揮発性半導体メモリのスクリーニング装置を示すブロック図である。

【図2】本発明に用いた不揮発性半導体メモリのセル構造を示す図であり、(a)はセル構造の概念図を、(b)はメモリアレイの概念図を示す。

【図3】本発明のスクリーニング方法を示すフローチャートである。

【図4】本発明の消去可能回数と消去時間を測定するフローチャートである。

【図5】本発明の消去時間および消去回数の測定結果を示すグラフである。

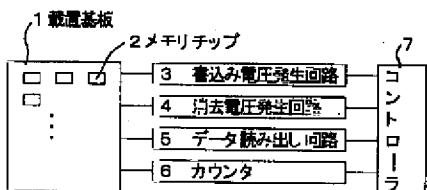
【図6】本発明の消去可能回数と消去時間との関係を示すグラフである。

【図7】従来のスクリーニング方法であるしきい値電圧を使用した不揮発性半導体メモリのヒストグラムである。

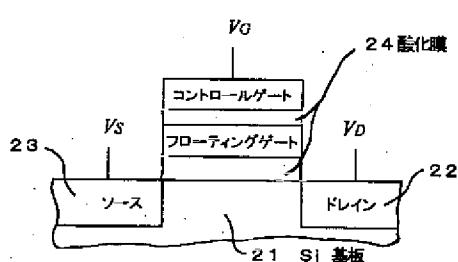
【符号の説明】

- 1：載置基板
- 2：メモリチップ
- 3：書き込み電圧発生回路
- 4：消去電圧発生回路
- 5：データ読み出し回路
- 6：カウンタ
- 7：コントローラ

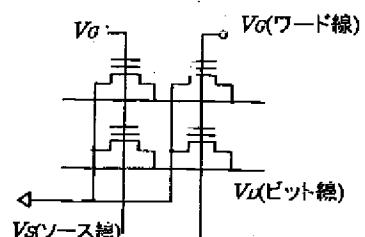
【図1】



【図2】

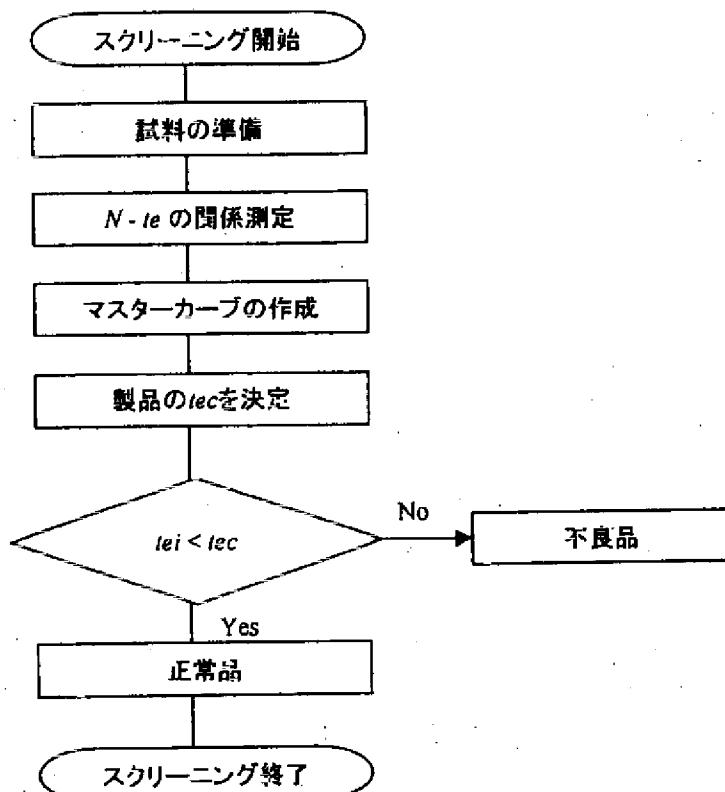


(a)

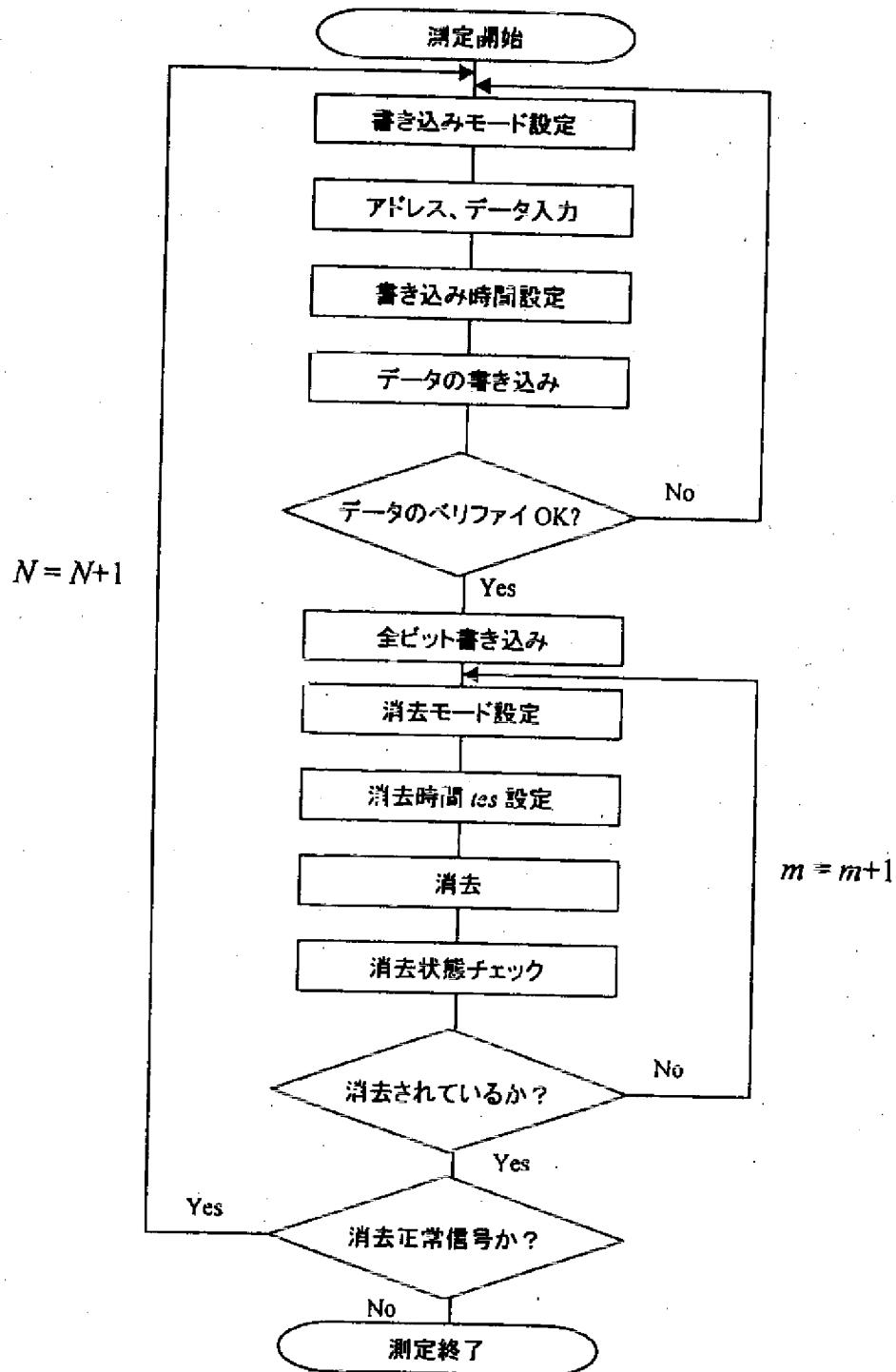


(b)

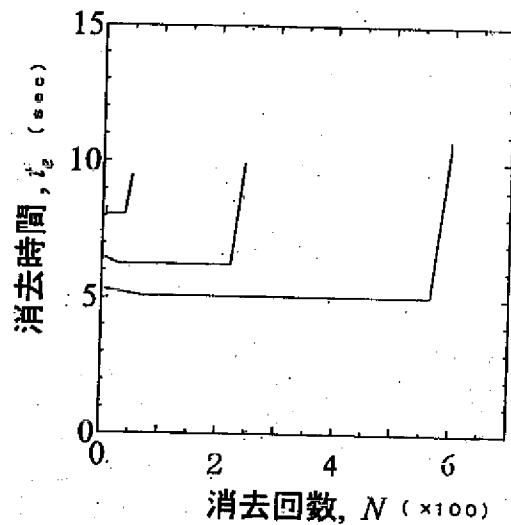
【図3】



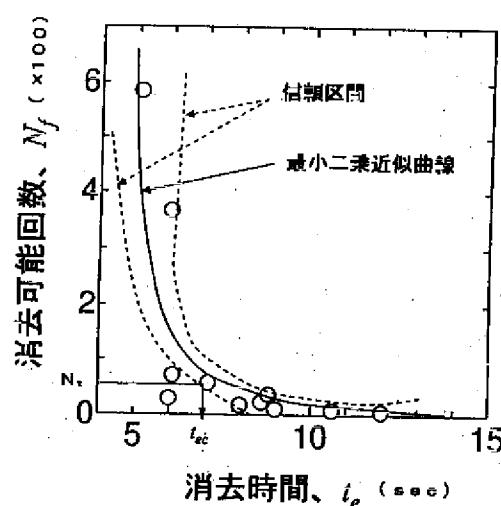
【図4】



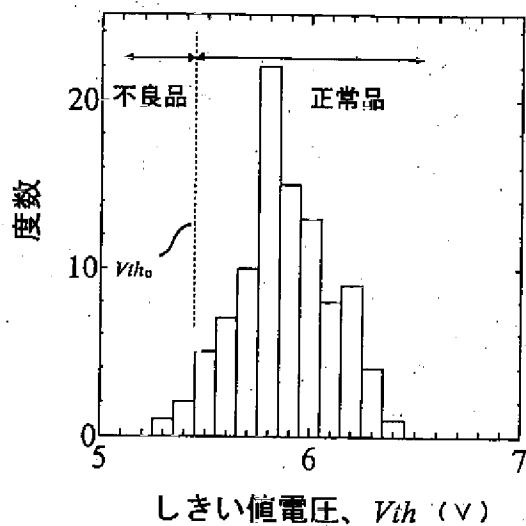
【図5】



【図6】



【図7】



フロントページの続き

F ターム(参考) 2G032 AA07 AB01 AB02 AC03 AD05  
 4M106 AA01 AA04 BA14 CA26  
 5B003 AA05 AB05 AD03 AD04 AE04  
 5L106 AA10 DD22 DD25 DD35  
 9A001 BB03 JJ45 KK37 LL05